



SOFTWARE SPECIFICATION
FOR
SMT6045

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Document No. D006045S-spec	Revision 0.3	Date 10/07/2005	Page 1 of 11
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APPROVAL PAGE

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DOCUMENT HISTORY

Date	Initials	Revision	Description of change
10/04/05	B.V.	0.1	Initial Draft
10/06/05	B.V.	0.2	Expanded considerations section, and test requirements
10/07/05	B.V.	0.3	Further clarifications in considerations, diagram of SMT148 operation, added considerations for passive carrier boards. Introduced the concept of an SMT6045-CP adapter.

TABLE OF CONTENTS

1.	SCOPE.....	5
1.1.	INTRODUCTION	5
1.2.	PURPOSE.....	5
1.3.	APPLICABILITY	5
2.	APPLICABLE DOCUMENTS AND REFERENCES.....	6
2.1.	APPLICABLE DOCUMENTS	6
2.1.1.	<i>External Documents</i>	6
2.1.2.	<i>Internal documents</i>	6
2.1.3.	<i>Project Documents</i>	6
2.2.	REFERENCES	6
2.2.1.	<i>External documents</i>	6
2.2.2.	<i>Internal documents</i>	6
2.2.3.	<i>Project documents</i>	6
2.3.	PRECEDENCE.....	6
2.4.	COPYRIGHT.....	6
3.	ACRONYMS, ABBREVIATIONS AND DEFINITIONS.....	7
3.1.	ACRONYMS AND ABBREVIATIONS	7
3.2.	DEFINITIONS.....	7
4.	REQUIREMENTS.....	8
4.1.	PRIME ITEM DEFINITION	8
4.2.	PRIME ITEM CHARACTERISTICS.....	8
4.3.	CONSIDERATIONS FOR HARDWARE COMBINATIONS.....	9
4.3.1.	<i>Considerations for SMT148 Operation</i>	9
4.3.2.	<i>Considerations for Passive Carrier Board Operation</i>	10
4.3.3.	<i>Considerations for FPGA Module Operation</i>	10
4.3.4.	<i>Considerations for the class library and .dll interface</i>	10
4.4.	DOCUMENTATION	11
5.	QUALIFICATION REQUIREMENTS.....	11
5.1.	QUALIFICATION TESTS	11
6.	NOTES	11

1. SCOPE

An interface to Sundance embedded hardware via USB2.0 is proposed.

1.1. INTRODUCTION

Sundance DSP designs and implements modular hardware components consisting of reconfigurable hardware (FPGA), programmable DSP and high-speed sampling analog-to-digital components for a variety of customers and application areas. A typical Sundance system consists of a TIM module and a TIM carrier board.

Most applications use PCI or PC-104+ carrier boards to interface to the HOST PC. For these applications, SMT6025 and SMT6035 are available which provide device drivers and class libraries for interfacing to the modules. Embedded applications built upon the (non-PCI) SMT118, SMT148 and SMT180 currently cannot provide a high speed I/O¹ capability to a host except if tethered to a compatible PCI carrier board installed in the HOST PC.

Sundance DSP has been considering this problem for some time, and proposes to develop an adapter that interfaces the SDB (and SHB in 16-bit mode) to a USB2.0 device port.

1.2. PURPOSE

The purpose of this document is to define the requirements and specifications of the driver for the USB adapter designated as the software package SMT6045. The purpose of the software is to be able to interface to any Sundance module which provides an SDB (or SHB via SMT517/SMT518).

1.3. APPLICABILITY

- Sundance TIM-40 Hardware Modules
- Sundance TIM-40 Carrier Boards
- SMT6025
- SMT6045-X (CP/SDB/SHB to USB Adapter Board)

¹ Greater than 20MB/sec sustained throughput.

Document No. D006045S-spec	Revision 0.3	Date 10/07/2005	Page 5 of 11
--------------------------------------	------------------------	---------------------------	--------------

2. APPLICABLE DOCUMENTS AND REFERENCES

2.1. APPLICABLE DOCUMENTS

2.1.1. External Documents

TBD

2.1.2. Internal documents

D006045S_impl.doc

D006045S_veri.doc

2.1.3. Project Documents

Statement of Work for Sundance DSP Inc. - System Development and Drivers

NASA Technical Specification

2.2. REFERENCES

2.2.1. External documents

TBD

2.2.2. Internal documents

D006045H_spec.doc (SDB/SHB to USB Adapter Board Specifications)

D006045H_impl.doc

D006045H_veri.doc

2.2.3. Project documents

TBD

2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

2.4. COPYRIGHT

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Document No. D006045S-spec	Revision 0.3	Date 10/07/2005	Page 6 of 11
--------------------------------------	------------------------	---------------------------	--------------

3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1. ACRONYMS AND ABBREVIATIONS

ADC	Analog to Digital Converter
CCS	Texas Instruments Code Composer Studio
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
GUI	Graphic User Interface
GUID	Global Unique Identifier
RSL	Sundance RocketIO Serial Link
SDB	Sundance Digital Bus
SHB	Sundance High Speed Bus
SLB	Sundance LVDS Bus
TIM	Texas Instruments Module
USB	Universal Serial Bus

3.2. DEFINITIONS

4. REQUIREMENTS

4.1. PRIME ITEM DEFINITION

The product is a middleware software component that interfaces HOST applications to Sundance hardware.

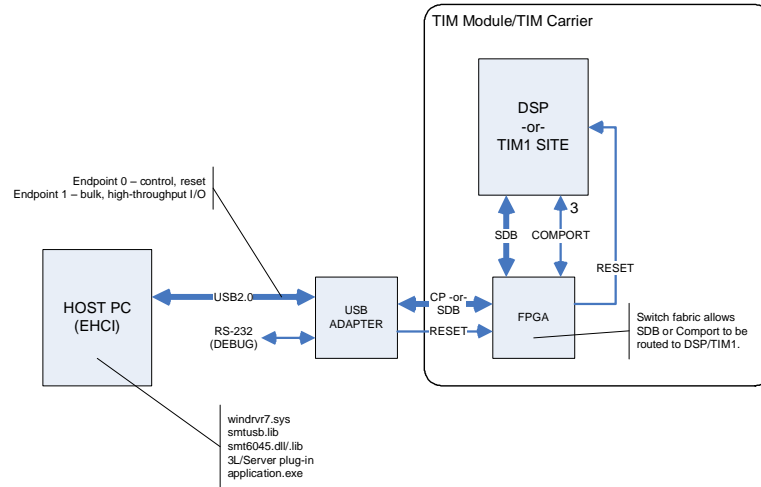


Figure 1 – HOST I/O Pipeline

The software will enable communication and control between Sundance embedded devices and the HOST over USB2.0. The I/O flow occurs between the HOST and the adapter over two endpoints. The control-type endpoint configures the USB adapter and supports vendor specific control. The bulk-type endpoint supports high-throughput data transfer.

4.2. PRIME ITEM CHARACTERISTICS

The SMT6045 software driver must have the following characteristics:

- Initialize/Close the USB connection.
- Perform Input/Output of high-throughput data over the USB connection.
- Manage multiple USB adapters.
- Terminate any pending transfer requests.
- Perform a target system reset.
- Support the 3L/Diamond server by installing a link driver, according to the server extension model.
- Provide a set of reference applications to demonstrate the operation of the software drivers.
- Provide a set of test applications to verify the operation of the software drivers.

4.3. CONSIDERATIONS FOR HARDWARE COMBINATIONS

4.3.1. Considerations for SMT148 Operation

When operating SMT6045 with the SMT148 embedded carrier, the SMT6045-SHB adapter and an SMT511-series cable must be used².

Another consideration when using the SMT148 regards the switch fabric firmware on the FPGA fitted on the board. In order to provide the system reset and system load functionality, the firmware must undergo a revision. If the firmware is not revised, then the functionality of SMT6045 will be limited to high-throughput data I/O only. There are two reasons for this requirement:

1. Reset must be communicated to the SMT148. Current FPGA firmware will not interpret the reset signal from the SMT6045-SHB adapter and will ignore it.
2. The external SHB must be connected to TIM1 comport 3, in order to emulate the existing Sundance assumption that the HOST interface is always connected to the root module's comport 3.

The switch fabric implemented in the FPGA of the SMT148 can route data streams to the SHB from a variety of sources. However, the only connections to the FPGA from the modules are comport links, which operate at approximately 20MB/sec (the limit of the comport specification when driving through connectors, etc.). In order to realize higher throughput transfers (the SMT6045-SHB adapter can saturate the USB2.0 bus); a second adapter may be connected directly to the SHB port of a module.

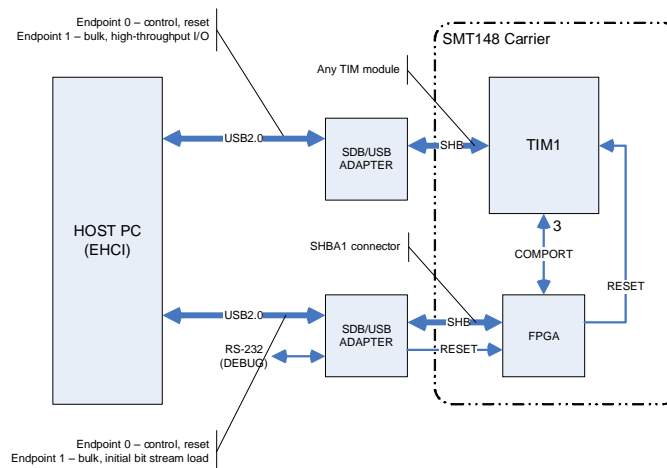


Figure 2 - Example Data Flow for SMT148

This arrangement allows for system control and program loading to occur through the carrier board FPGA and high-throughput I/O to occur directly to and from the TIM module site.

² The SMT6045-SDB, an SMT510-series cable and an SMT517 adapter may be used, but this would prevent the placement of a module on site 4. Only the SMT517 applies in this case, as the SMT518 (right-hand model) would collide with JP12.

4.3.2. Considerations for Passive Carrier Board Operation

Some users may choose to use TIM modules in an embedded configuration on passive carrier boards such as the SMT118 and SMT180. In such cases it is convenient to have the control, initial program load and high-throughput I/O occur over the USB2.0. There are two options:

1. Use the SMT6045-CP adapter and an SMT502 cable to provide access to the buffered comport which is installed on all Sundance carrier boards.
2. Use the SMT6045-SHB adapter and an SMT511 cable to attach directly to the “root” module.

For configuration 1, the “root” module requires no modification. In configuration 2, the “root” module firmware requires modification in order to support program load via the SHB and to recognize the reset signal driven by the SMT6045-SHB adapter. This modification can be made to the boot loader of the (DSP) module; the change involves expanding the window of valid inbound application load connections to include comport *and SHB*. In addition, firmware to recognize the reset signal from the SMT6045-SHB adapter can be incorporated into the FPGA for the module.

4.3.3. Considerations for FPGA Module Operation

SMT6045 is unable to initialize the FPGA directly if the adapter is connected to the SHB port of an FPGA module. This is because the FPGA must already be configured with a bit stream before the SHB port is active. However, placing FPGA modules onto a suitable carrier board (such as a revised SMT148) is possible and will allow for system loading.

When a system is composed of all FPGA modules, then a multi-stage loading process is recommended. This process first loads the bit stream for the root FPGA module. This FPGA contains a data I/O state machine which sequences the sending of the configuration bit streams to the next set of FPGA modules, etc. This process is outside of the scope of SMT6045, but any HOST software which uses SMT6045 will be able to implement such a multi-stage boot load.

This is no different than the existing situation, wherein the root FPGA module is configured by the HOST first. Subsequent FPGA modules must be configured by switching the incoming bit stream(s) from the HOST through the root FPGA to the rest of the FPGA modules in the network.

4.3.4. Considerations for the class library and .dll interface

The low-level interface to the USB subsystem is sufficiently different from the existing PCI-based system support library (smtdrv.dll), that a new .dll is developed.

The new .dll will expose a streamlined, native interface to the functionality of the high-throughput I/O capability via a zero-copy buffer management interface. This interface will not interfere with existing software defined to use smtdrv.h (SMT6025), and the two may be used together.

The class library will provide a compile-time switch to allow the functional equivalence of SMT6025 (using the identical API for the class IFHw) to be implemented by the SMT6045 .dll. In this way, SMT6045 will remain source code compatible with existing applications implemented under SMT6025.

Document No. D006045S-spec	Revision 0.3	Date 10/07/2005	Page 10 of 11
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4.4. DOCUMENTATION

The following documents shall be produced and reviewed as part of the design process:

- Software Design Description
- Software Source Code
- Software Verification containing:
 1. Test Requirements
 2. Test Procedures
 3. Test Results

5. QUALIFICATION REQUIREMENTS

5.1. QUALIFICATION TESTS

Test programs will be developed to verify the operation of all I/O and control components. This includes all host I/O communication channels, and inter-module communication channels such as the low-speed comport and the high-speed SHB, etc. Each component will be tested as follows:

- Basic operation (unit test)
- Loopback operation (data integrity test)
 - HOST to driver
 - HOST to USB Adapter
 - HOST to FPGA (carrier board or module as appropriate)
 - HOST to DSP (root processor)
- Performance characterization
- HOST CPU utilization for I/O

6. NOTES

TBD

Document No. D006045S-spec	Revision 0.3	Date 10/07/2005	Page 11 of 11
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