# TIM COMPATIBLE PARALLEL PROCESSING WITH THE TMS320C6X FAMILY

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## *ABSTRACT*

*Sundance Multiprocessor Technology has produced two compatible TMS320C4x Texas Instruments Modules, TIM's, incorporating the TMS320C6x DSP. This gives the C6x a seamless parallel processing capability compatible with the TMS320C4x family of processors. The paper discusses communication port speeds and channel I/O methods and mixed family processing techniques and code distribution.*

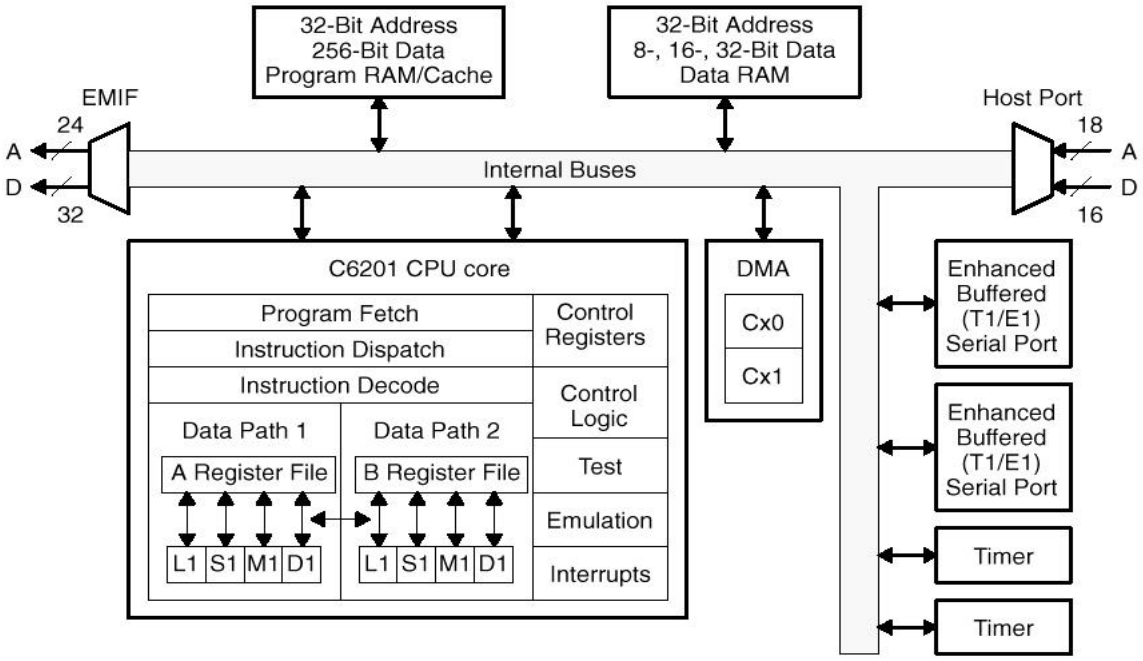
## *1. TMS320C6x Processor*

The C6201 is a 200MHz fixed point RISC processor and the C6701 is a 167MHz floating point RISC processor. With eight functional units, including two multipliers and six arithmetic logic units the CPU can execute up to eight instructions per cycle. All instructions are conditional so reducing time for branching. The memory maybe accessed via 8, 16 or 32bit wide instructions for efficient memory support, with 40-bit arithmetic options. Saturation and normalisation allow safer integer arithmetic operations on the C6201 with the C6701 supporting single cycle floating point multiplication. The device includes 65KBytes of internal memory, four channels for direct memory access, two serial ports, a host-port interface (HPI) and two 32-bit timers.

## *2. TIM-40 Specification*

Several United Kingdom customers of the Texas Instruments TMS320C4x, required a cost effective parallel processing module to improve system designs. In collaboration with Texas Instruments they defined the TIM-40 module specification [1].

Specifically targeted at the C40, with its six communication ports, enabling



hypercube multiprocessing [2][3][4], the specification does not exclude the use of other processors. Special-to-type modules, such as ADC's, (figure 2), DAC's, SCSI controllers, re-configurable FPGA's, (figure 3), image processing frame grabbers, from being implemented.

Restrictions come in the form of pin-outs, power limits or mechanical properties. The module is intended to be reusable on different architectures, to be plugged into motherboards to build homogeneous systems. TIM modules maybe double, triple

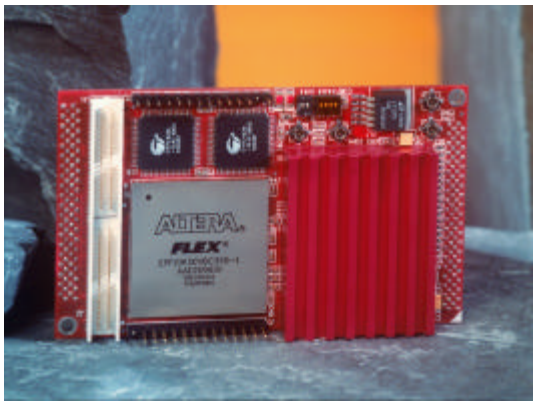



**Figure 2 Single Sized 80MBs$^{-1}$ ADC TIM with 200MBs$^{-1}$ Sundance Data Bus Connectors**

or quadruple width dependent upon the backplane.

The TIM modules are provided with a support environment in the form of motherboards. The motherboards provide the environment for the modules to operate and communicate with others and the host machine. Larger systems maybe built by utilising multiple motherboards.

The motherboards are available for a variety of backplanes, (PC-ISA, VME, PCI, CompactPCI, VXI, PMC). There are no restrictions on the backplane, only on the module sites. The result is, users investments are in the processing and special-to-type modules which make the system.

The TIM specification allows for an ID ROM to be installed. This allows software to determine the location of resources or the type of hardware it is running on and information on the

**Figure 1 TIM Mother Board Populated with 4 C6x SMT331 TIM's**

manufacturer.

Building modules, which are TIM compliant, allows systems to be rapidly configured using combinations of TIM's and motherboards. This eliminates hardware


**Figure 3 Re-configurable FPGA TIM with SDB**

development or prototyping boards for many applications.

## 3. C6x TIM

For the SMT331, Figure 3, or SMT332 TIM to communicate with C4x TIM's, four compatible communication ports are provided. These communication ports interface to any standard 'C4x.

The communication ports can operate in two modes. The first mode allows the C6x to transfer data to the port directly using a polling technique. Alternatively the

C6x's DMA controller is set to trigger via an external interrupt, (INT4..7).

As the C6x is running at 200MHz or 167MHz, the option of selecting a motherboard clock is disabled.

From figure 4 it can be seen the C6x TIM presents the same communications ports as a TMS320C44 processor TIM.

## 4. Implementation

To enable the connection of communication ports to C4x TIM's, compliant ports have been implemented onto the C6x TIM using an FPGA. The C4x communication ports are implemented in an FPGA [5]. These are then mapped on the asynchronous memory space of the C6x, Table 1.

### 4.1 Global Bus Compatibility

Part of the TIM specification defines an optional global expansion connector. This expansion connector allows the TIM's CPU access to host motherboard resources. The C6x TIM's implements a fully compliant TIM global connector through the use of an EPLD. The global bus transactions are synchronised to the C6x's clock. A maximum block size of 64k words may be accessed at once and a page register can be used to access the upper 15 address bits.

### 4.2 Program Download and Debugging

A cross compiler and development environment on a host system is used for building executables and system programs. The host may then be used to download the programs and interact with the DSP system via the communication port or the global bus address that interface to the motherboard.

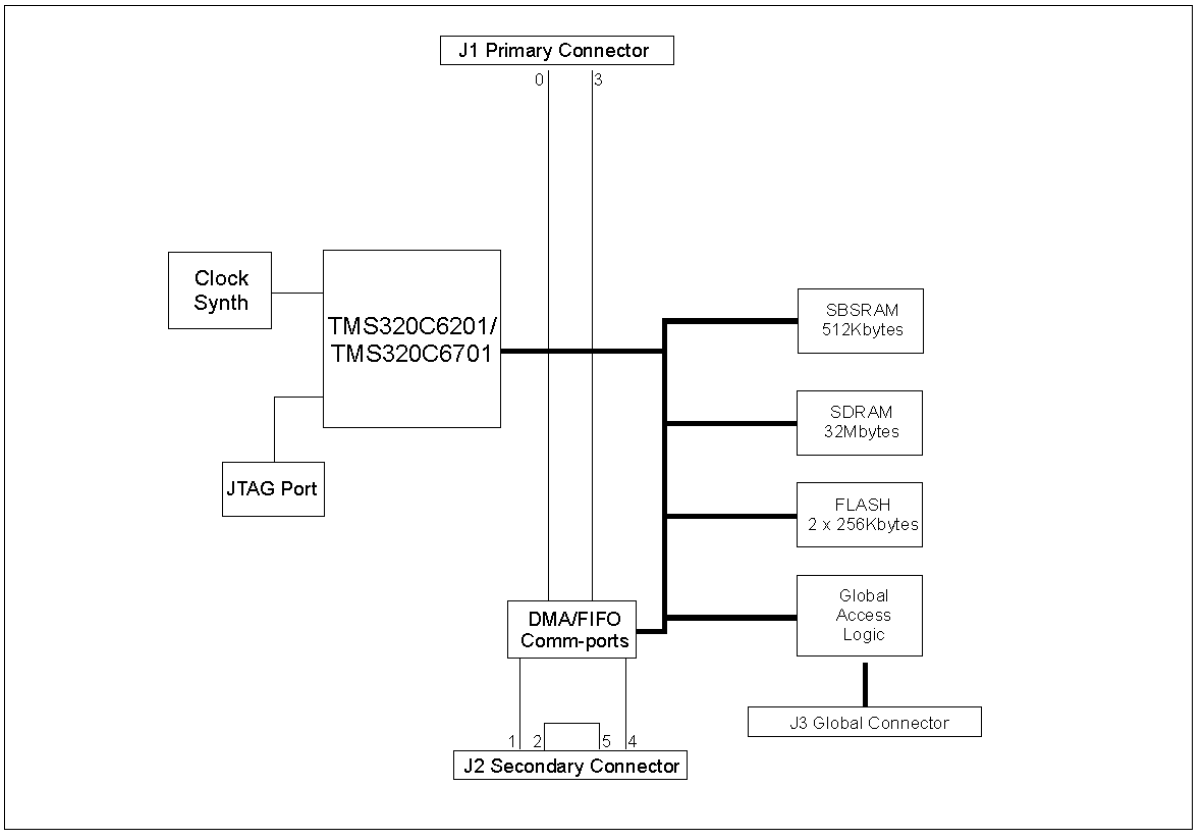



**Figure 4 SMT331 TIM Block Diagram**

Debugging on the Texas Instruments C4x and C6x family of processors is facilitated using a boundary scan technique, IEEE 1149.1 standard refereed to as the JTAG [6]. On the host the debugger interface [7] communicates with a JTAG controller on the motherboard. Multiprocessor debugging is available in differing windows and all

internal registers and memory are available for evaluation and, if allowed, modification.

### 4.3 None TIM Spec Voltage Supplies

The TIM specification does not stipulate 3.3v or 2.5v supplies that are required by the C6x processors. To overcome this, a 3.3v supply from the motherboard is presented onto two diagonally opposite TIM mounting holes. This is then fed into an on TIM regulator to derive the 2.5v core voltage for the C6x.

Table 1 SMT331 Memory Map

| Starting Address | RESOURCE | Refer to |
|---|---|---|
| 0000 0000 | Internal Program RAM | |
| 0001 0000 | Reserved | |
| 0040 0000 | External Memory Space CE0<br>512kb SBSRAM | SBSRAM |
| 0140 0000 | External Memory Space CE1<br>256kb Flash | Flash |
| 0150 0000 | External Memory Space CE1<br>FPGA program pin control | Communications Ports |
| 0160 0000 | External Memory Space CE1<br>FPGA internal registers (comm ports) | Communications Ports |
| 0170 0000 | External Memory Space CE1<br>Global bus access | Global Expansion |
| 0178 0000 | External Memory Space CE1<br>Global bus page register | Global Expansion |
| 0180 0000 | Internal Peripherals | |
| 01C0 0000 | Reserved | |
| 0200 0000 | External Memory Space CE2<br>16Mb SDRAM | SDRAM |
| 0300 0000 | External Memory Space CE3<br>16Mb SDRAM | SDRAM |
| 0400 0000 | Reserved | |
| 8000 0000 | Internal Data RAM | |
| 8001 0000 | Reserved | |
| 8040 0000 | Reserved | |

## *5. Results*

### 5.1 Communication Port Speeds

With the present FPGA, the communication ports achieve speeds over 17MBs$^{-1}$ between a C4x and the C6x. Communication between two C6x's is over 22MBs$^{-1}$.

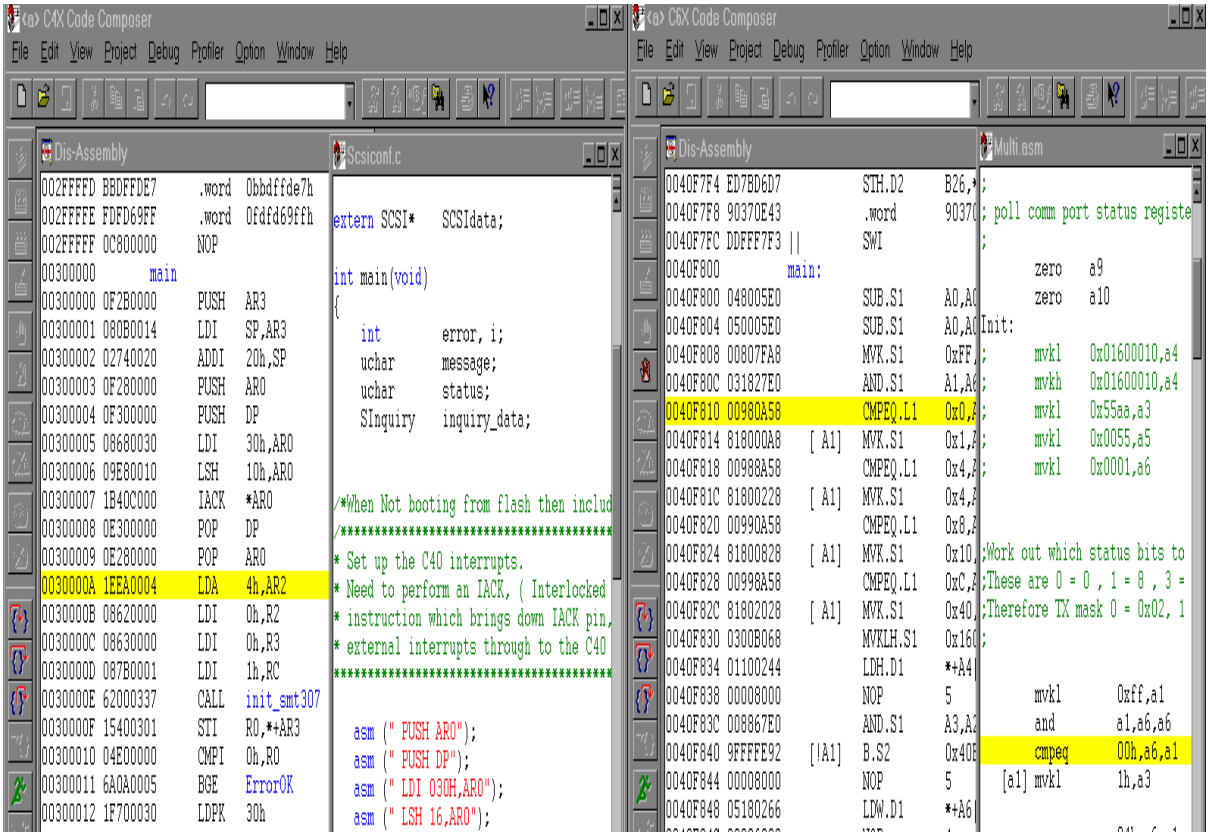
### 5.2 Multi and Mixedprocessor Program Downloading

To facilitate C6x multiprocessor downloading and execution, each TIM program must be compiled into a compatible COFF file. On the host each COFF file is decoded and all executables are concatenated into a byte stream which can be written directly to the C4x compatible communication port. The form of the uploading to the C6x has been designed to be completely C4x compatible [8]. This requires padding of the C6x data which is byte aligned compared with the C4x word alignment. This form of compatibility allows the inclusion of C4x applications in the upload code and seamless mixing of the processor families. In this way all of the present C4x TIM's available maybe used without modification of their code, (although limited standard I/O calls to the host are implemented).

### 5.3 Mixed Processor Debugging

The Texas Instruments 8990 JTAG controller with Code Composer debugger from Go DSP has been used on this research. It is possible to ignore a processor

in the JTAG chain by setting up the number the clocks used to pass through the chip. Both the C4x and the C6x processors require the same number of clocks, so by running two versions of the Code Composer on the host it is possible for one instantiation of the Code Composer to bypass the C4x's and the other to bypass the C6x's. Both programs use the same settings in the 8990 controller so simultaneous debugging of two different families of chip is possible, as can be seen here.




## 6. Application

A system has been built consisting of a set of SMT331 C6x TIM's, each fed data from an SMT349 80MHz ADC. The results are output over the communication ports to a 'C44 DSP on an SMT348 DAC TIM. This 'C44 then feeds a DAC that is outputting at 30MHz.

This system is being used successfully for research into software radio and beamforming [9].

## 7. Further Research

Improvements in performance of the C4x compatible communication ports will be implemented by use of a higher speed FPGA. Special C6x communication ports are being developed which are predicted to increase performance to at least 40-50MBs$^{-1}$.

Presently two real time kernels are being ported to the C6x TIM, DNA Enterprise's ASP and 3L's Diamond. 3L's Diamond already exists on the 'C4x TIM's and with use of the multiprocessor downloading capability previously described, has enabled previous real time C4x systems to be used without modifying any of their configuration or code.

The porting of the two Real Time kernels will afford real time multithreaded/multitasking capabilities on the C6x TIM's.

A new TIM, SMT332 Figure 5, has been designed with the Sundance Data Bus, SDB, high speed interface. These connect directly to other high speed DAC's and

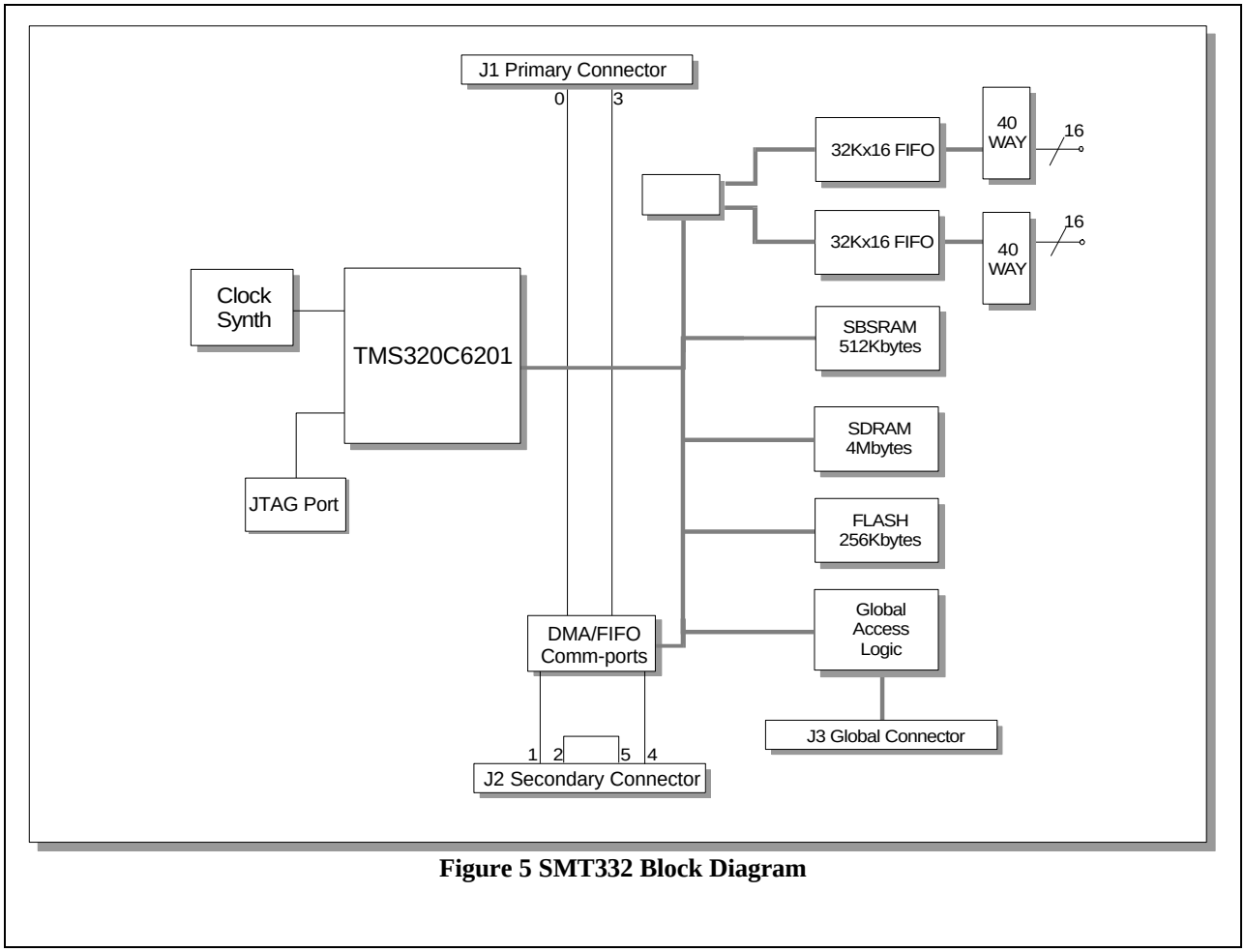



**Figure 5 SMT332 Block Diagram**

ADC's, typically the SMT359 clocked at 40MHz 10bit ADC or the SMT348 DAC.

A new motherboard with global connectors on all TIM sites, SMT350, will allow shared memory program management schemes and very high speed data distribution. This also allows the host to communicate with all TIM sites and have data DMA'ed directly into it's memory from any TIM.

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